

# **ENCODING ALGORITHM FOR CROSSTALK EFFECT MINIMIZATION USING ERROR CORRECTING CODES**

**SOUVIK SINGHA<sup>1</sup> & G. K. MAHANTI<sup>2</sup>**

<sup>1</sup>Department of Computer Science & Informatics, Bengal Institute of Technology and Management, Santiniketan,  
West Bengal, India

<sup>2</sup>Department of Electronics and Communication Engineering, National Institute of Technology, Durgapur,  
West Bengal, India

## **ABSTRACT**

In this paper we present an analysis of crosstalk effects on buses implementing error correction codes. Crosstalk between adjacent wires on the bus may create a significant portion of delay with increasing die size and shrinking wire dimensions. Wires are becoming longer and more resistive and at the same time clock frequencies are rising. If two adjacent wires have simultaneous rising transition, both transitions speed up and a hold violation is possible. Similarly a rising transition on one wire can cause a neighboring wire to falsely transit and lead to a logic fault. In particular, we present an implementing error correcting codes for analysis of crosstalk effects on buses using hamming single error correcting codes. We give algorithms for generating optimal bus encodings and provide a general construction method for a practical class of codes using extra one even parity bit. Encoding and decoding circuits are given for specific codes. We first report the results of an analysis and then using hamming single error correcting codes to reduce the interference in DSM buses.

**KEYWORDS:** Bus Encoding, CODEC Algorithm, Error Correction, Parity Check Code, Single Error Correction